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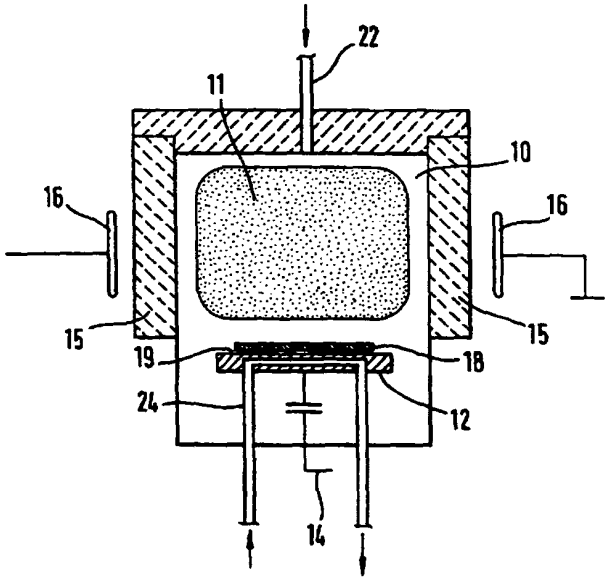
(54) Abstract Title
Anisotropic plasma etching of trenches in silicon by control of substrate temperature

(57) In the anisotropic plasma etching of trenches in a silicon layer or wafer, the relative etching speed in trenches having different width or depth-width ratios is adjusted by controlling the temperature of the silicon substrate. The temperature of the substrate 18 in a plasma chamber 10 is controlled within the range -100°C to +200°C by flowing refrigerant in line 24 through the substrate electrode 12. A helium gas cushion 19 provides thermal coupling between the electrode and the substrate. The temperature across the substrate may have local variations provided by differential heating or cooling. Other means of temperature control include nitrogen cooling, electric heating or using a Peltier element.



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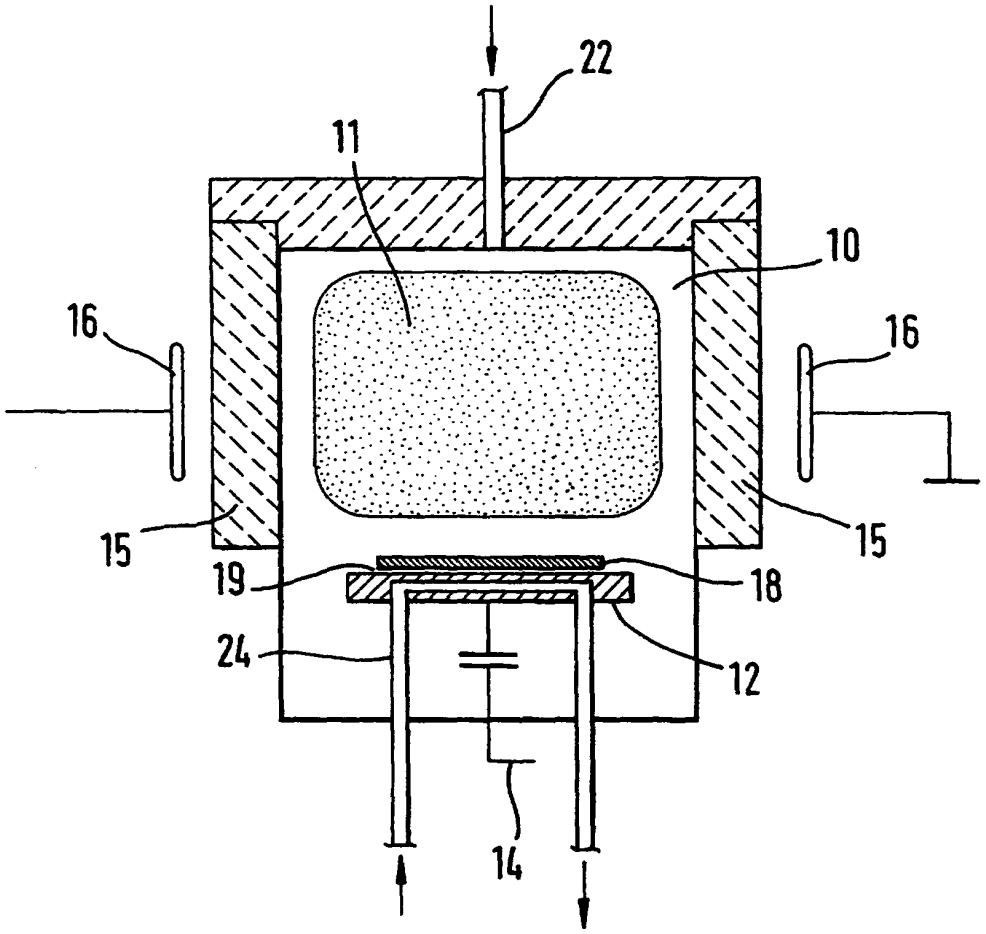
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A Process for Adjusting the Etching Speed in the Anisotropic Plasma Etching of Lateral Structures

Prior Art

The invention is based on a process for anisotropic plasma etching in silicon according to the introductory clause of the Main Claim.

Such a process is known for example from DE 42 41 045 wherein, for silicon deep etching, deposition steps are performed in alternation with inherently isotropic etching steps. During the deposition steps a deposition gas yielding polymer-forming monomers and preferably consisting of octafluorocyclobutane C_4F_8 or perfluoropropylene C_3F_6 is exposed to a high-density plasma, for example a PIE plasma (propagation ion etching plasma) or a ICP (inductively coupled plasma) resulting in the formation of $(CF_2)_n$ radicals which build up a teflon-like film of $(CF_2)_n$ on the side walls of etched silicon structures and in part also on the etching base. During the actual etching steps, an etching gas yielding fluorine radicals and consisting for example of sulfur hexafluoride SF_6 is likewise exposed to a high-density plasma by means of PIE or ICP excitation, whereby a high density of fluorine radicals and at the same time ions is produced. Fluorine radicals give rise to a spontaneous, inherently isotropic etching of silicon. With suitably selected process parameters, the ion flow to the wafer surface exposes the etching base of polymer material, causes the side wall film precipitated during the deposition steps to be driven forwards down into the etched trenches, and provides for the local protection of the silicon side walls during the progressive, inherently isotropic etching step.

In the process proposed in the unpublished DE Application 197 06 682, anisotropic silicon etching is achieved in that a side wall passivation, compatible

with the etching chemistry of fluorine radicals from sulfur hexafluoride, is performed by the simultaneous deposition of SiO_2 from silicon tetrafluoride SiF_4 and oxygen using a high-density plasma source. By the addition of oxide-consuming reactive substances, this passivation is selectively removed by ionic action on the etching base of the structures to be etched. In both of these processes, as in all other types of RIE processes, the so-called "RIE-lag" or "microloading" effect occurs, i.e. with increasing depth, narrow structures are etched more slowly than wider structures. The fundamental causes of these effects are transport phenomena in the narrow trenches and in the trenches having a large depth-width ratio, which impede the transportation of reaction products from the etching reaction out of the trenches and the supply of fresh etching species to the etching base. The overall effect of these phenomena is that narrow and deep structures, i.e. trenches having a large depth-width ratio (aspect ratio), are etched more slowly than wide and flat structures having a small aspect ratio. This effect can be desirable or undesirable. It is undesirable when structures of different width are to be etched to the same depth in equal time periods, as otherwise structural loss and inaccurate structural dimensions can occur. The microloading or RIE lag effect is desirable when wide structures are to be etched to a greater depth than narrow structures in the same time period.

The object of the invention is to improve upon existing processes for the anisotropic plasma etching of laterally defined structures in a silicon layer, such that purposive relative adjustment of the etching speed in trenches of different width and trenches having different depth-width ratios is possible, and in particular also a virtually equal etching speed is achieved.

Advantages of the Invention

Compared to the prior art, the process according to the invention comprising the characterising features of the Main Claim has the advantage that it permits the

purposive relative adjustment of the etching speeds in trenches of different width and trenches having different depth-width ratios in the anisotropic plasma etching of laterally defined structures in a silicon layer or a silicon wafer. Particularly advantageously, virtually equal etching speeds can also be achieved in the foresaid trenches of different width and trenches having different depth-width ratios.

A further advantage of the process in the case of special applications consists in adjusting the temperature of the silicon layer or silicon wafer such that the etching of wide trenches takes place at a defined, high etching speed and the etching of narrow trenches takes place at a defined, distinctly lower etching speed so that, with simultaneous etching of the entire silicon layer, different etching depths are attained by controlling the etching time.

By means of the easily modifiable and easily controllable parameter of the temperature of the silicon layer or silicon wafer and a corresponding adaptation of the etching cycle time, the RIE-lag factor - i.e. the ratio of the etching speed in wide trenches and in trenches having a small depth-width ratio to the etching speed in narrow trenches and trenches having a large depth-width ratio - can be adjusted within a wide range. In particular, the RIE lag factor can be set at any desired value in the range from approximately 2:1 to approximately 1:1, whereby an optimal adaptation to the particular problem is achieved.

In the case of a RIE lag factor of 1:1, the special advantage is achieved that the silicon layer is etched to the same depth overall in equal time periods and the etching can thus lead for example to buried structures like a buried sacrificial oxide without running the risk of significant overetching in wide trenches or not reaching the buried structures in narrow trenches.

The process according to the invention has the further advantage that, by means of a small number of calibration tests, with defined, otherwise identical process

parameters, by varying the temperature of the silicon layer it is possible to determine the etching speeds in silicon which are typical for the apparatus construction, for example using an etching mask with predefined recesses of different width, in that trenches of differing width are etched for a defined time period and the depths obtained are measured. One thus obtains a calibration curve of the etching speeds in the silicon layer as a function of the layer temperature and the trench width.

Advantageous further developments of the process according to the invention are possible by means of the measures described in the sub-claims. For example the etching speed can be influenced via further parameters such as the ICP plasma power, etching gas concentration, ion density, gas flow, pressure, substrate bias power and the like. Expediently, the layer temperature is generally set between 100°C and 200°C. However, it can also be higher or lower according to the requirements in special applications in dependence upon the power and form of the heating and cooling device for adjusting the temperature of the silicon layer and upon the etching gas used.

Drawing

Exemplary embodiments of the invention will be explained in detail making reference to the drawing and in the following description. The single Figure illustrates a schematic construction of an etching device known per se which can be used for the process.

Exemplary Embodiments

The Figure represents a section through an etching chamber 10 with ceramic walls 15 in which is arranged a substrate electrode 12 connected to a high-frequency

input 14 (shown only in part) via which a substrate bias power flow can be input. The etching chamber 10 is wound with a ICP coil 16, for example comprising one turn, by means of which, via a high-frequency generator (not shown), a high-density, inductive plasma 11 is produced in the etching chamber 10. A silicon layer 18, which for example can consist of a silicon substrate in the form of a wafer, is arranged on the substrate electrode 12. The process gases are supplied via a gas inlet 22. Reference is made to DE 42 41 045 C1 for further details of the process. The temperature of the silicon layer 18 is adjusted via a refrigerant cycle 24 (shown only in part) containing for example a dielectric liquid with good electric insulation properties, such as for example deionised water, a fluorocarbon (manufacturer: 3M; type: PF 5070 or FC 77) or alcohol, which circulates between the substrate electrode 12 and a refrigerating machine (not shown). The Figure is to be understood merely as an example of a construction forming the basis of various technical embodiments with which the skilled man will be familiar. The refrigerant cycle 24 enables the temperature of the silicon layer 18 to be adjusted via the temperature of the substrate electrode 12 at least in the range from -100°C to +200°C. The thermal coupling of the silicon layer 18 to the substrate electrode 12 can take place for example via an interposed helium gas cushion 19.

Further possibilities of influencing the temperature of the silicon layer 18 consist for example in the use of a heating plate beneath the substrate electrode 12, cooling by means of a cooling finger and using liquid nitrogen which is brought into contact with the silicon layer 18 so that thermal conduction occurs, heating conductors which are integrated into the substrate electrode 12 and for example are electric, or the provision of a Peltier element beneath the substrate electrode 12 or integrated into the substrate electrode 12.

The process for adjusting the layer temperature does not itself form the subject of the invention, but merely the fact that a desired temperature of the silicon layer 18 is attained from the exterior, substantially independently of the other process

parameters. In an advantageous further development of the invention based on a corresponding objective, via a geometric arrangement of different heating and cooling elements it is also possible to adjust different temperatures at different locations of the silicon layer 18, so that locally varying etching speeds are attainable by way of an additional parameter. In any case, it is necessary for the skilled man to perform a measurement and calibration of the temperature and temperature distribution occurring on the surface of the silicon layer 18 on the basis of simple experiments following the attainment of thermodynamic equilibrium. This can take place for example by recording a calibration curve as a function of the heating and cooling power or for example by arranging a thermo-element on the surface of the silicon layer 18.

To counter the precipitation of sulfur in the exhaust gas region of the etching apparatus (e.g. in the turbomolecular pump, the fore-pump and the exhaust gas pipes), in addition to the theory of DE 42 41 045 C1, a constituent of 5% to 25% oxygen is added to the process gas during the etching steps. This eliminates the sulfur formation arising from the etching steps using the etching gas SF_6 as the sulfur is oxidized to form volatile sulfur-oxygen compounds. In place of the etching gas SF_6, advantageously it is also possible to use the etching gas chlorotrifluoride ClF_3, bromotrifluoride BrF_3 or iodine pentafluoride IF_5, optionally diluted with an inert gas such as for example helium, as even with a relatively low-intensity plasma excitation these etching gases emit very large quantities of free fluorine radicals required for the silicon etching without harmful precipitations of solids.

The crux of the process according to the invention is the surprising observation that processes for example of the type according to DE 42 41 045 C1 and DE Application 197 06 682 react to the temperature of the silicon layer 18 in that the etching speed in wide trenches decreases at a low layer temperature whereas the etching speed in narrow trenches remains virtually unaffected by the temperature

of the silicon layer 18. It is thus possible for the RIE-lag factor or microloading factor to be adjusted during the etching via the layer temperature substantially independently of the other process parameters and to be adapted to the particular objective. In particular, the etching speed in narrow trenches can be virtually fully matched to that in wide trenches so that, for example, no overetching occurs in wide structures while the etching in narrow structures advances up to an etch stop.

In the following, on the basis of the process published in DE 42 41 045 C1, details will be given of the process management of the process according to the invention in the form of exemplary embodiments in which oxygen is additionally added to the process gas during the etching steps to avoid sulfur precipitations in the exhaust gas region of the etching apparatus.

In the case of process management according to DE 42 41 045 C1 and the use of an additional oxygen constituent in the process gas during the etching steps, the following process parameters are set for example at room temperature with ICP excitation.

Exemplary Embodiment 1:

Deposition steps:

Gas flow and process gas	100 sccm C_4F_8
Pressure:	8 to 15 mTorr
High-frequency power of the ICP-coil:	800 W
No substrate bias power	
Duration of the deposition steps:	in each case 5 s

Etching Steps:	
Gas flow and process gas:	130 sccm SF_6 and 20 sccm O_2
Pressure:	17 to 22 mTorr
High-frequency power of the ICP-coil:	800 W
Substrate bias power:	8 W
Duration of the etching steps:	in each case 8 s
Temperature of the silicon layer:	+35°C
Profile form:	vertical profile
Typical Etching Speeds:	
Narrow trenches (approx. 2 µm width):	2 µm/min
Wide trenches (> 60 µm width):	3 µm/min

By the selection of different process parameters, such as for example high-frequency power, pressure and gas flow, it is also possible to attain different etching speeds, in particular of 5 µm/min or more. In the case of Exemplary Embodiment 1, the RIE lag factor is 1.5 : 1.

If, in the process according to DE 42 41 045 C1 modified by the addition of oxygen to the process gas during the etching steps, the temperature of the silicon layer 18 is reduced, the process tends to become more ion-induced. Consequently the etching reaction is determined less by the quantity of available fluorine radicals than by the quantity of ions which remove the etching base polymer. Therefore a reduction in the temperature of the silicon layer 18 to -30°C leads for example to etching speeds according to Exemplary Embodiment 2 with a RIE-lag factor of approximately 1:1.

Exemplary Embodiment 2:

Deposition Steps:	
Gas flow and process gas:	100 sccm C_4F_8
Pressure:	8 to 15 mTorr
High-frequency power of the ICP coil:	800 W
No substrate bias power	
Duration of the deposition steps:	in each case 5 s
Etching Steps:	
Gas flow and process gas:	130 sccm SF_6 and 20 sccm O_2
Pressure:	17 to 22 mTorr
High-frequency power of the ICP coil:	800 W
Substrate bias power:	8 W
Duration of the etching steps:	in each case 13 s
Temperature of the silicon layer:	-30°C
Profile form:	vertical profile
Typical Etching Speed:	
Narrow trenches (approx. 2 µm width):	2 µ/min
Wide trenches (> 60 µm width):	2 µ/min.

Also in this case it is easily possible to achieve different etching speeds, in particular of 5 µm/min or more, by the selection of different process parameters, such as for example high-frequency power, pressure and gas flow.

As stated, a change in the temperature of the silicon layer 18 in the process according to the invention leads to a change in etching speed as a function of the

trench width. Thus with a fixed etching depth, following the determination of the etching speed, the etching times to be set must in each case be adapted via appropriate calibration tests easily implementable by the skilled man.

A change in the etching cycle time in the case of process management of the type according to DE 42 41 045 C1 corresponds to a change in the scavenger cycle time and scavenger gas flow in the case of process management according to DE Application 197 06 682. Accordingly, the above exemplary embodiments are also transferrable to this process management, in the case of which the supply and discharge of heat can take place for example in accordance with the described embodiments.

Claims

1. A process for the anisotropic plasma etching of laterally defined structures with trenches of different width and/or with different depth-width ratios of the trenches in a silicon layer (18), wherein differences in etching speed occur in the case of trenches of different width or trenches having different depth-width ratios, characterised in that the etching speeds in the trenches of different width and/or in the trenches having different depth-width ratios are adjusted via the temperature of the silicon layer (18).

2. A process according to Claim 1, characterised in that the etching speeds in trenches of different width and/or in trenches having different depth-width ratios are approximately equal.

3. A process according to Claim 1, characterised in that the etching speeds in trenches of different width and/or in trenches having different depth-width ratios are adjusted differently to one another and differ in particular by a factor of up to two.

4. A process according to Claim 1, characterised in that the temperature of the silicon layer is adjusted from -100°C to 200°C, in particular from -50°C to 100°C.

5. A process according to Claim 1, characterised in that for the attainment of predetermined etching depths, the etching speeds occurring in the trenches as a function of the temperature of the silicon layer (18) are used to determine the required etching time.

6. A process according to Claim 1, characterised in that locally varying etching speeds in trenches differing in width and/or in the trenches having

different depth-width ratios are adjusted via temperatures locally varying within the silicon layer (18).

7. A process according to Claim 1, characterised in that the etching speed is influenced by further parameters, such as plasma power, etching gas concentration, ion density, gas flow, pressure, substrate bias power and the like.

8. A process according to Claim 1, characterised in that the etching speed is determined as a function of the temperature in trenches of different width and/or in the trenches having different depth-width ratios by at least one calibration test.

9. A process for the anisotropic plasma etching of laterally defined structures substantially as hereinbefore described with reference to the accompanying drawing.

The Patent Office

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INVESTOR IN PEOPLE

Application No: GB 9921482.7 **Examiner:** Graham Russell
Claims searched: 1-9 **Date of search:** 22 December 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q):

Int Cl (Ed.6): H01L 21/3065

Other: Online: EPODOC, PAJ, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0729175 A1	(IBM) see column 1 lines 31-38	1,4
X	EP 0383570 A2	(HITACHI) see column 1 lines 18-34	1,4
X	US 5705029	(HITACHI) see column 4 line 14 - column 5 line 4	1,4
A	US 5637189	(XEROX) see column 2 lines 41-52	1
A	US 5605600	(IBM)	1
A	US 5362361	(SONY)	1
A	US 5147500	(HITACHI)	1
X	US 4943344	(HITACHI) see column 4 lines 26-43	1,4

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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